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MODULATION WAVEFORM TYPES

1. INTRODUCTION

Several basic pseudo-noise spread spectrum modulation approaches are considered as potential candidates for RF transmission over the ARPA Packet Radio Network. A comparison of these different modulation approaches is summarized in Figure 1. The modulation approaches considered are differentially coherent bi-phase PSK, differentially coherent quadri-phase PSK, coherent MSK, differentially coherent (DC) MSK, pseudo-orthogonal (PO) MSK and noncoherent (NC) 8'ARY MSK signalling. PSK and MSK refer to chip modulation, and coherency refers to bit modulation.

Each of these approaches will be examined with respect to their implementation and performance. Each approach considered is flexible in that the processing gain can be increased by using a larger number of chips per bit. Also, frequency hopping can be readily superimposed upon the pseudo-noise spread spectrum baseline concept.

Each approach is also shown implemented at both the modulator and demodulator with surface acoustic wave devices (SAWD). The ad-

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vantages and potential of these devices appear very great, particularly with respect to considerations of fast acquisition, low power and size requirements. These factors are especially important for the hand-held packet radio transceiver.

2. PSK MODULATION/DEMODULATION

2.1 Differentially Coherent Bi-Phase Modulator/Demodulator

The differentially coherent bi-phase PSK modulation approach was discussed in the Packet Radio Temporary Note #33. The modulator differentially encodes the data. Each time a logic 1 bit is to be transmitted, the bit sequence is inverted. However, each time a logic 0 bit is to be transmitted, the code sequence remains the same. One implementation of the modulator is shown in Figure 2. For the baseline system, spread factors of 100 are assumed; therefore, a data bit "1" transmits a sequence of 100 phase modulated chips with each chip either 0° or 180°. The data sequence from the source may be represented by the following sequence

1 0 1 1 0 1 0 0 . . .

After differentially encoding the data, the sequence becomes

1 1 0 1 1 0 0 0 1 . . .

The impulse generator drives the 100 tap SAWD with either a positive or negative impulse. The output of the SAWD at the point where the taps are summed is

$$s(t) = \sum_{i=1}^{100} d_{101-i} \cos (W_o t+\phi) \; [u(t-(i-1)T_c) - u(t-iT_c)]$$

where d_i is either $\pm$ 1 depending upon the sign of the chip and T_c is the chip duration.

An alternate DPSK modulator is shown in Figure 3. The chip sequence for a data bit is exclusive-ored with the differentially encoded data bit. The impulses are generated on a chip basis yielding a phase modulated carrier at the SAWD output. A positive impulse may correspond to a 0° phase shift and a negative impulse corresponds to a 180° phase shift.

One of the shortcomings of bi-phase PSK modulation is its spectral density response which, as shown in Figure 22, rolls off as $1/f^2$ or 20 dB per decade.

The DPSK demodulator is shown in Figure 4. It is a matched filter at the IF. As shown, a single SAWD is matched to the chip sequence and the same chip sequence delayed one data bit time. The outputs of the taps are summed both for the present received bit and the previously received bit. This summing operation takes place right in the SAWD. The sum and difference is obtained from the two outputs. These are envelope detected, compared and the output is sampled. The sample time is established by the preamble detector and the sampling occurs at the peak of the baseband pulse. The sign of the sampled signal determines whether the data bit is a "1" or a "0".

Maximum Likelihood Detection

This type of detection assumes ideal bit timing and ideal sampling of the correlation waveform peak. Ideal timing is never achieved for bit timing. For non-ideal bit timing, Figure 5 shows the result of loss of signal envelope detection versus timing error. Figure 6 shows the loss of signal/noise (E_b/N_o) as a function of

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number of chips per bit with timing error τ as a parameter for T_B of 10μs (100 KBPS data rate).

Hence, for N = 100 and 10ns bit timing error for 100 KBPS data, a 1 dB loss of E_b/N_o is incurred. Note that 10ns out of 10μs bit period is .36° of timing accuracy and requires a 100 MHz clock if a counter is allowed to freerun from a master clock. A 1.0° error (28ns) results in 3 dB loss. Thus, bit timing requirements are quite important for spread spectrum maximum likelihood detection.

Gated Peak Store Detection

An alternate method of data detection is achieved by sampling the SAWD matched filter output by a timing window that is $2T_c$ (T_c = chip interval) wide, storing the peak value during that timing window and making a bit decision at the end of the timing window. This method greatly alleviates the bit timing problems that the maximum likelihood detection requires since ideally, bit timing of only T_c accuracy is required (100ns for N = 100).

It is estimated that this form of detection degrades performance by .5 dB (for a $2T_c$ window case) from the ideal timing. A $2T_c$ window is suggested for two reasons. One is that a $2T_c$ window is easy to generate. The second is that intuitively, a window equal in width to the correlation peak width would result in best performance.

Thus, for much easier timing requirements, a .5 dB performance penalty results. Hence, performance of DCPSK with $P_e = 10^{-5}$ requires E_b/N_o = 10.9 dB rather than 10.4 dB. A suggested method of implementing the detector is shown in Figure 7.

2.2 Differentially Coherent Quadri-Phase PSK Modulator/Demodulator

Quadri-phase modulation has certain advantages over bi-phase modulation. One is that the timing requirements are less severe since the symbols are twice as long as the chips. Another is that the bandwidth requirements are less as shown in Figure 22.

An implementation of the modulator is shown in Figure 8. The demodulator for quadri-phase PSK is similar to that shown in Figure 4 for bi-phase demodulation. An orthogonal channel is required which is phase shifted 90° from the other channel. This can be achieved by a 90° phase shift of the two SAWD outputs (A and B). These 90° phase shifted outputs are input to a hybrid, and the sum and difference of the outputs are envelope detected and compared in the same manner as the other channel.

Maximum likelihood detection and gated peak store detection criteria discussed for bi-phase apply for quadri-phase, except symbol intervals ($T_c/2$) must be used in the applicable equations and curves. Note that there are 2 chips per symbol for quadri-phase.

3. MSK MODULATION/DEMODULATION

An alternate approach to PSK signalling is sometimes referred to as Minimum Shift Keying (MSK). It is a two orthogonal channel amplitude weighting PSK modulation scheme. The in-phase and quadrature phase carrier channels are staggered by one chip and shaped with orthogonal cosine weightings of two chip length.

This is illustrated in Figure 9. To achieve a constant envelope signal, the quadrature channel is added to the in-phase channel as shown in the MSK waveform diagram. Also shown is the resultant phase and frequency for the example chip stream. Phase transitions can occur at the null points of each sub-channel. This property results in phase continuity of the MSK waveform.

This property produces increased attenuation of the higher signalling frequencies. Its spectral density rolls off as $1/f^4$, or 40 dB per decade as shown in Figure 22.

3.1 Coherent MSK Modulator/Demodulator

Several approaches to MSK modulation/demodulation are being considered. The first of these approaches is termed coherent MSK. A data bit "1" consists of a sequence of 100 chips and a data bit "0" consists of the same sequence with inverted signs. Figures 10 and 11 illustrate two implementation techniques for the modulator. In Figure 10 the data source determines the sign of the impulse driving the SAWD. The input transducer has a cosine pulse weighting and has a duration of 2 chip periods. The SAWD has 100 taps, each tap corresponding to one of the chips. The even taps are summed for one MSK subchannel and its output is phase shifted 90°. The odd taps are summed for the other subchannel. The two outputs are then added together yielding the MSK signal. The signal can be represented mathematically as follows:

$$s(t) = \sqrt{2P}\left[\cos(W_o t+\phi)\sum_{k=0}^{49} d_{2k+1}\cos p\,\frac{\pi}{2T}(t-2kT) + \sin(W_o t+\phi)\sum_{K=0}^{49} d_{2k+2}\sin p\,\frac{\pi}{2T}(t-2kT)\right]$$

where cosine pulse "cosp" is defined by:

$$\text{cosp}\ \frac{\pi t}{2T} = \cos\frac{\pi t}{2T}\ [u(t+T) - u(t-T)]$$

and sine pulse "sinp" is defined by:

$$\text{sinp}\ \frac{\pi t}{2T} = \sin\frac{\pi t}{2T}\ [u(t) - u(t-2T)]$$

and the chip interval is given by T.

The IF output is then up converted and amplified for transmission. The summing of the odd and even taps is accomplished in the SAWD. It may be feasible to also do the phase shifting in the SAWD. However, further investigation in this area is required.

An alternate approach to the modulator is shown in Figure 11. The SAWD is impulsed at the chip rate. The sign of the impulse determined by the exclusive output of the SAWD generates a cosine weighted pulse which exists for two chip periods. The impulse sign determines carrier phase in the cosine pulse.

The demodulator is shown in Figure 12. The demodulation process is coherent. The matched filter demodulator is identical to the modulator discussed above (Figure 10) except that the tap sequence is reversed. The summing of the two SAWD output results in an amplitude modulated carrier which is the correlation function. This IF signal must be sampled at exactly the right time because the phase of the IF carrier contains the information. Hence, near coherence is required which can be achieved by use of a phase lock loop which encloses the surface wave detector.

In a half-duplex application, it is possible to share the SAWD between the transmitter and receiver (c.f. Figures 10 and 12). The complexity of the switches must be compared to the complexity of a SAWD.

3.2 Differentially Coherent MSK (DC MSK) Modulator/Demodulator

To alleviate the severe timing requirements of the coherent MSK demodulator, an alternate approach is considered. With this approach the data is differentially coded prior to being modulated as was discussed in Paragraph 2.1. A data bit from the source is differentially encoded with the previously encoded data bit. The remaining part of the modulator (Figure 13) is identical to the modulator discussed above for the coherent MSK approach. The modulator can also be constructed using the 2 chip SAWD as shown in Figure 11. The only additional requirement is the differential encoding of the data source output.

A differentially coherent MSK demodulator is shown in Figure 14A. Two SAWD's are shown. One is a 10μsec (1 bit) MSK demodulator and the other is a 10μsec delay. The demodulator coherently detects the present data bit and delays the previously detected bit for one bit interval. These two outputs are then multiplied coherently and low pass filtered yielding a baseband output whose sign determines the data bit. The bit timing derived from the preamble is used to sample the mixer output and recover the data. A second DC MSK demodulator is shown in Figure 14B. The concept is the same as the DPSK demodulator shown in Figure 4. The advantage is the elimination of phase coherent mixer.

The two types of detection discussed for DPSK signalling are also applicable for MSK signalling. The effect of timing errors upon

the loss of signal energy is shown in Figure 15. For MSK signals the correlation function is not triangular as it is for PSK signals but is a smooth function as shown in Figure 15. For small timing offsets the loss factor is less than it is for 4-phase PSK signalling. For timing errors in excess of 1/4 of a chip the loss factor is less for 4-phase PSK signalling. With 2-phase PSK signalling, any and all timing offsets will be worse than 4-phase PSK or MSK.

3.3 Pseudo-Orthogonal MSK (PO MSK) Modulator/Demodulator

Another MSK modulation approach is illustrated in Figures 16 and 17. To modulate the pseudo-orthogonal signals requires the selection of one of two chip sequences. These chip sequences have approximately zero cross-correlation. In Figure 16 a data bit "1" selects, for example, the upper SAWD for the generation of the MSK signal and the data bit "0" selects the lower SAWD. In Figure 17 the data bit selects the chip sequence which controls the impulse generator driving the MSK SAWD.

At the demodulator illustrated in Figure 18 the incoming signal is correlated by both SAWD's, each containing one of the chip sequences. Each SAWD is an MSK detector for a bit. One SAWD is matched to a data "1", the other SAWD is matched to a data "0". Each output is envelope detected and the output with the largest amplitude is selected. This approach requires two SAWD's each of 10μsec in length. The timing requirements are the same as those for the differentially coherent MSK demodulator. In this type of data detection, maximum likelihood detection and gated peak store detection may be used.

3.4 8'ARY MSK Modulator/Demodulator

Another signalling approach which yields a performance improvement over the approaches discussed above at low bit error probabilities is shown in Figures 19 and 20. The modulator utilizes 8 SAWD's. Each SAWD has 300 taps and the taps are arranged such that they correspond to the 300 chips for each code symbol. The cross-correlation between the eight 300 chip sequences is approximately zero. However, each code sequence has an autocorrelation function that has a large peak four chips wide and very low sidelobes. Three data bits from the source comprise a symbol and are used to select one of the eight chip sequences. For the chip rate in the channel to be 10 megachips per second requires 300 chips per symbol. Again, there is an input transducer for each of the SAWD's which has a cosine pulse weighting.

At the demodulator the IF signal is power split between eight SAWD's each of which is matched to one of the 300 chip sequences. Again, each is a matched filter for one of the eight possible 3 bit data sequences. The output of each filter is envelope detected and every symbol time the largest output is selected. The most likely bits are the three bits associated with the largest output. The timing requirements for this approach are more stringent than DC MSK since for 300 chips, the same correlation peak occurs. One of the drawbacks is the number of SAWD's required and the lengths of the SAWD's (30μsec). This can be alleviated in the modulator by using programmable SAWD's. The modulator could be implemented by using a programmable digital code generator driving a chip SAWD MSK generator.

4. PERFORMANCE COMPARISON

A probability of bit error performance comparison between the six modulation/demodulation approaches discussed above is shown in Figure 21. The chip rates in the channel are all the same. The comparison is made on the basis of probability of bit error (BER) versus the energy per bit to noise spectral density required to achieve a given error probability. For bit error probabilities in excess of 7×10^{-5}, coherent PSK or MSK is superior. For bit error probabilities less than 7×10^{-5}, 8'ARY MSK is superior. It requires .4 dB less energy per bit than coherent MSK at 10^{-5} BER.

Differentially coherent PSK and differentially coherent MSK have identical theoretical performance. At 10^{-5} BER their performance is 1 dB less than coherent MSK and 1.4 dB poorer than 8'ARY MSK. Pseudo-orthogonal (PO) MSK gives the poorest performance. Basically, this is because the correlation between the chip sequences is not positive N or negative N, but is either positive N or nearly zero. Hence, the signal detector space geometric separation between signals is not as great with the result of poorer performance. The performance of PO MSK is 3 dB worse than coherent DMSK as shown in the figure.

5. TRADEOFF PARAMETERS

Figure 1 contains some parameters which are important for deciding which modulation or signalling waveform approach is most desirable for the ARPA Packet Radio Network. The six modulation approaches are compared on the basis of performance. The best performance is denoted by 1 and the poorest performance is denoted by 5. These are qualitative indicators only.

The bandwidth utilization of the different modulation methods was also discussed above. The basic difference is between the PSK and MSK power spectrum for an equal chip rate. MSK has much lower out-of-band spectral energy and, hence, is superior where spectral containment is important. The PSK power spectrum rolls off at 20 dB per decade, whereas, the MSK spectrum rolls off at 40 dB decade. Quadri-phase PSK requires half the bandwidth of bi-phase PSK.

The timing requirements refer to the demands upon timing accuracy. Differentially coherent MSK and pseudo-orthogonal MSK have the least stringent timing requirements for small timing errors. 8'ARY MSK is more difficult because the slope of the correlation function per bit interval is greater. QPSK is superior for large timing errors. Bi-phase PSK is inferior for all timing errors. Coherent MSK requires the most accurate timing because one must sample the IF carrier in order to sense the sign of the data bit. To adequately recover the data from the coherent MSK modulated signal will require a phase lock loop.

The hardware limitations refer specifically to the device requirements relative to state-of-the-art technologies. For example, 10μsec SAWD's are relatively easy to make; whereas, 20μsec SAWD's are a little more difficult and 30μsec SAWD's require some extra development work. On this basis, coherent MSK is considered to have the fewest SAWD hardware limitations and 8'ARY MSK would have the most.

The judgments on the last three tradeoff parameters are more subjective and require more extensive investigation. The evaluation is based on first-pass engineering judgment.

The conclusions one might draw from such a tradeoff is that coherent MSK and differentially coherent MSK are the leading contenders. Coherent MSK has the problem of very accurate timing requirements since one must track the phase of the carrier for adequate detection. DC MSK circumvents this phase locking difficulty by coherently detecting two successive bit intervals. However, the price one pays is a slight performance degradation (≈1 dB). In actual practice, there will probably be .5 dB degradation due to phase tracking errors and jitter with coherent MSK.

Our recommendation at this time would be to assume differential coherent MSK as the baseline modulation approach.

TRADE OFF PARAMETERS / MODULATION TYPE	PERFORMANCE BER vs Eb/No @ 10^{-5} BER		BANDWIDTH UTILIZATION	TIMING REQUIREMENTS (BIT SYNC.)	SAWD LIMITATIONS	EQUIPMENT COMPLEXITY	ESTIMATED COST	EQUIPMEN SIZE
DIFFERENTIALLY COHERENT BI-PHASE PSK (2)	14	3	3	3	2	1	1	1
DIFFERENTIALLY COHERENT QUADRI-PHASE PSK (3)	16	3	2	2	3	2	2	2
COHERENT MSK (5)	20	2	1	5	1	4	3	4
DIFFERENTIALLY COHERENT MSK (1)	10	3	1	1	2	1	1	1
PSEUDO-ORTHOGONAL MSK (4)	17	4	1	1	2	3	3	3
8'ARY MSK (6)	22	1	1	2	4	5	4	5

EVALUATION SCALE 1 - MOST DESIRABLE
TO
5 - LEAST DESIRABLE

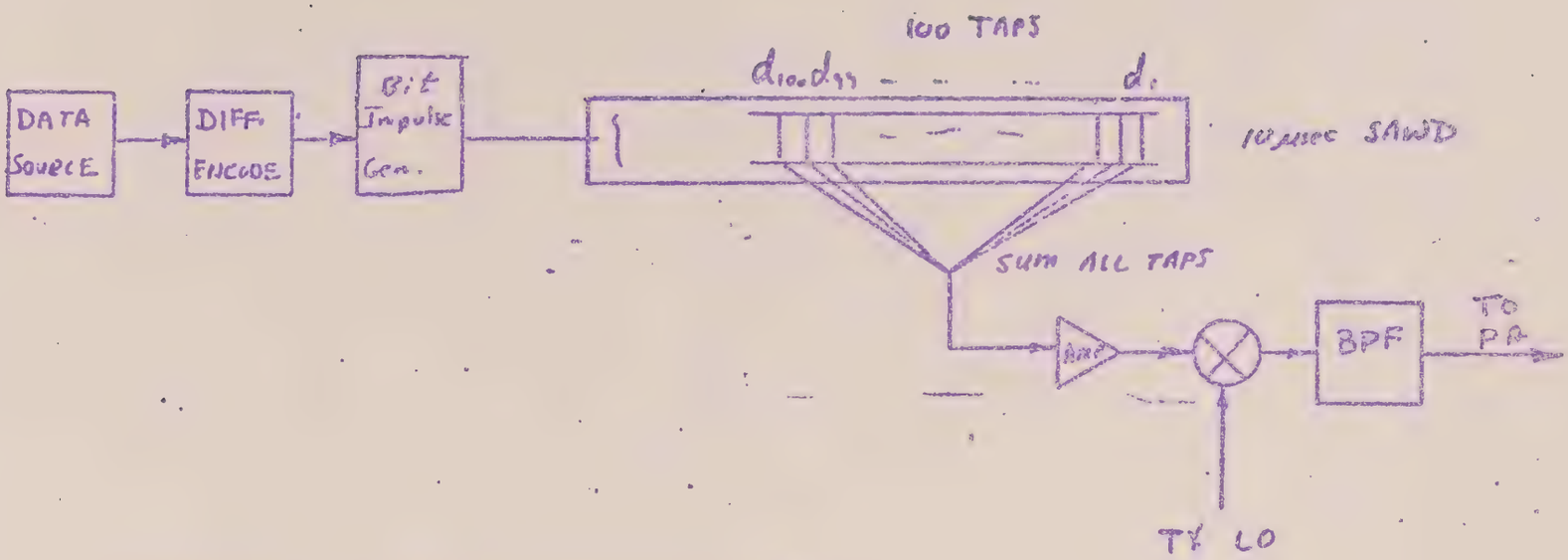


FIGURE 2 DPSK MODULATOR #1

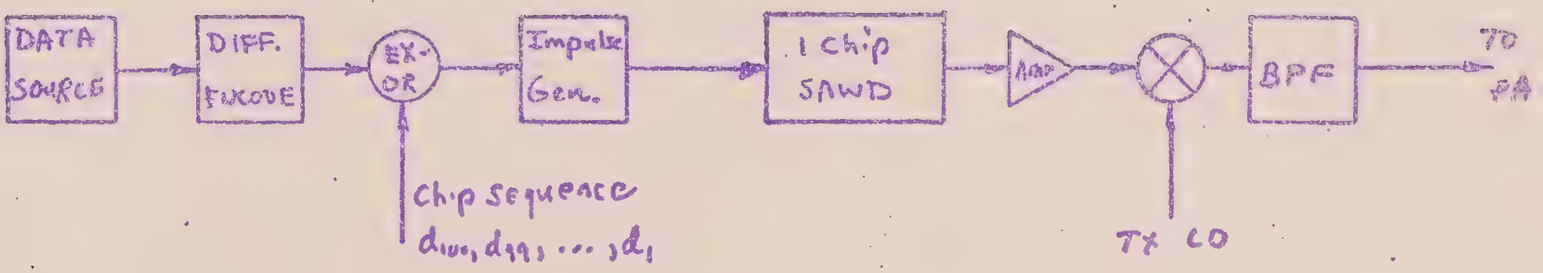


FIGURE 3 DPSK MODULATOR #2

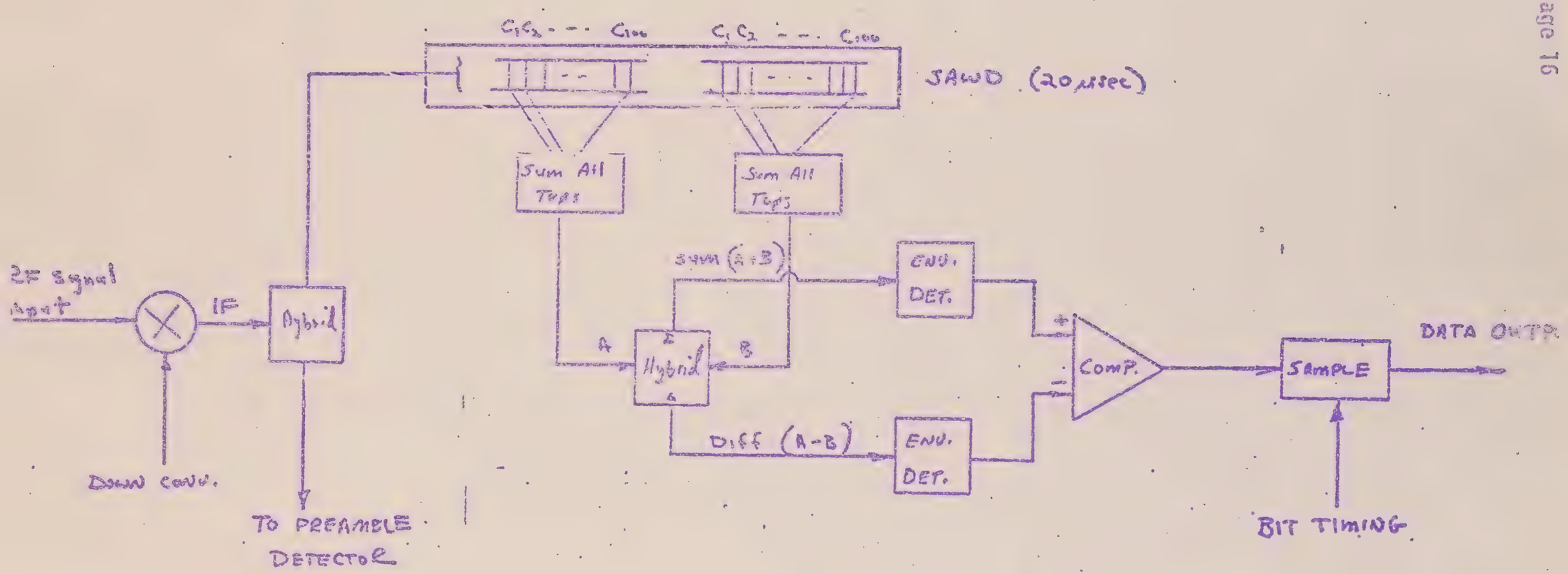
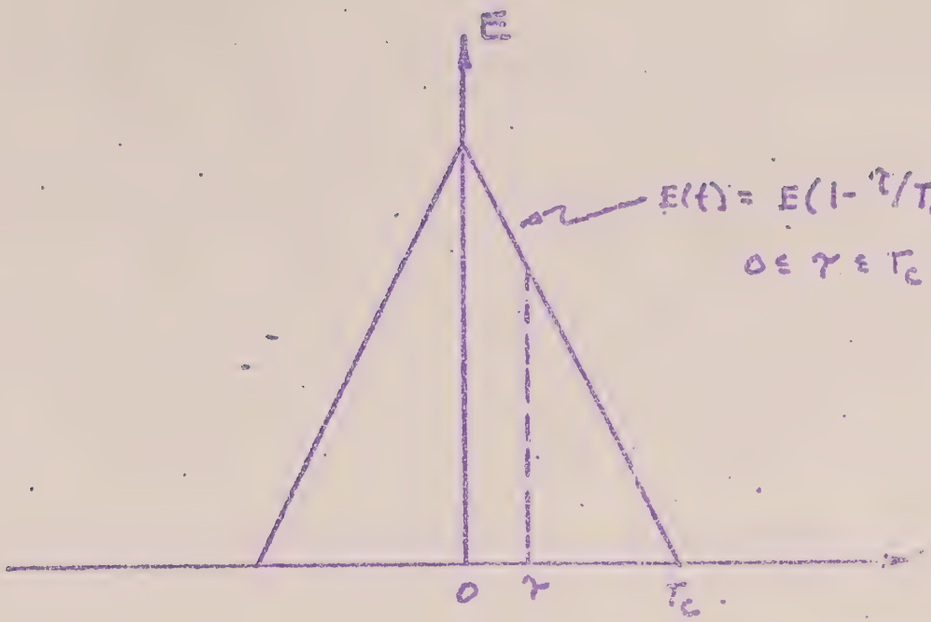


FIGURE 4 DIFFERENTIALLY COHERENT PSK DEMODULATOR



SIGNAL AT OUTPUT OF ENVELOPE DETECTOR

$$\text{LOSS FACTOR} = [1 - \tau/T_c]^2$$

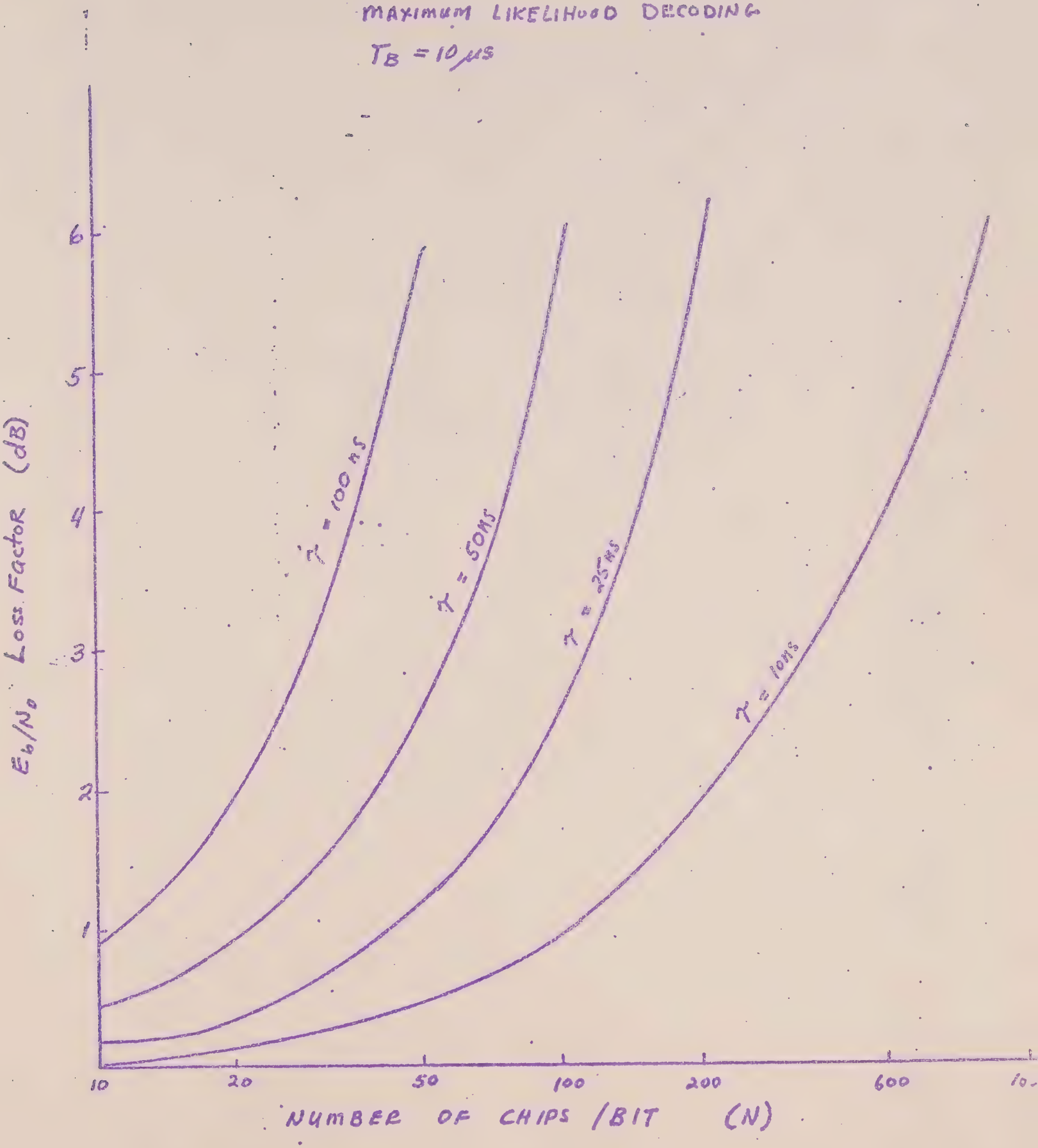
τ/T_c	LOSS FACTOR (dB)
0	0
.05	.45
.10	.92
.20	1.95
.30	3.10
.50	6.0

FIGURE 5 Effect of Timing Offsets to Maximum Likelihood Decoding

FIGURE 6 E_b/N_o Performance Loss Due to Timing offsets (τ)

MAXIMUM LIKELIHOOD DECODING

$T_B = 10\,\mu s$



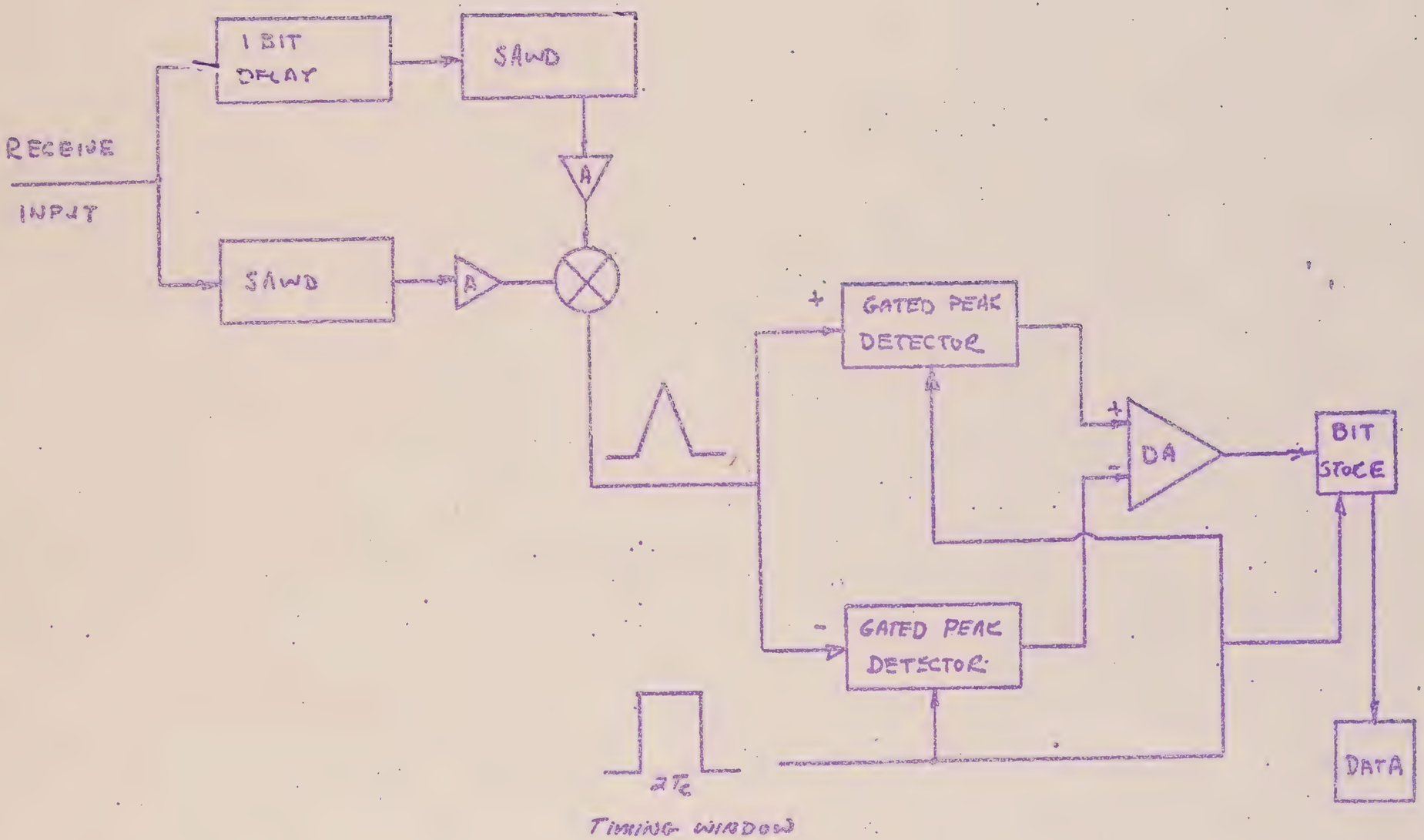


FIGURE 7 WINDOW PEAK SAMPLE & STORE DETECTOR

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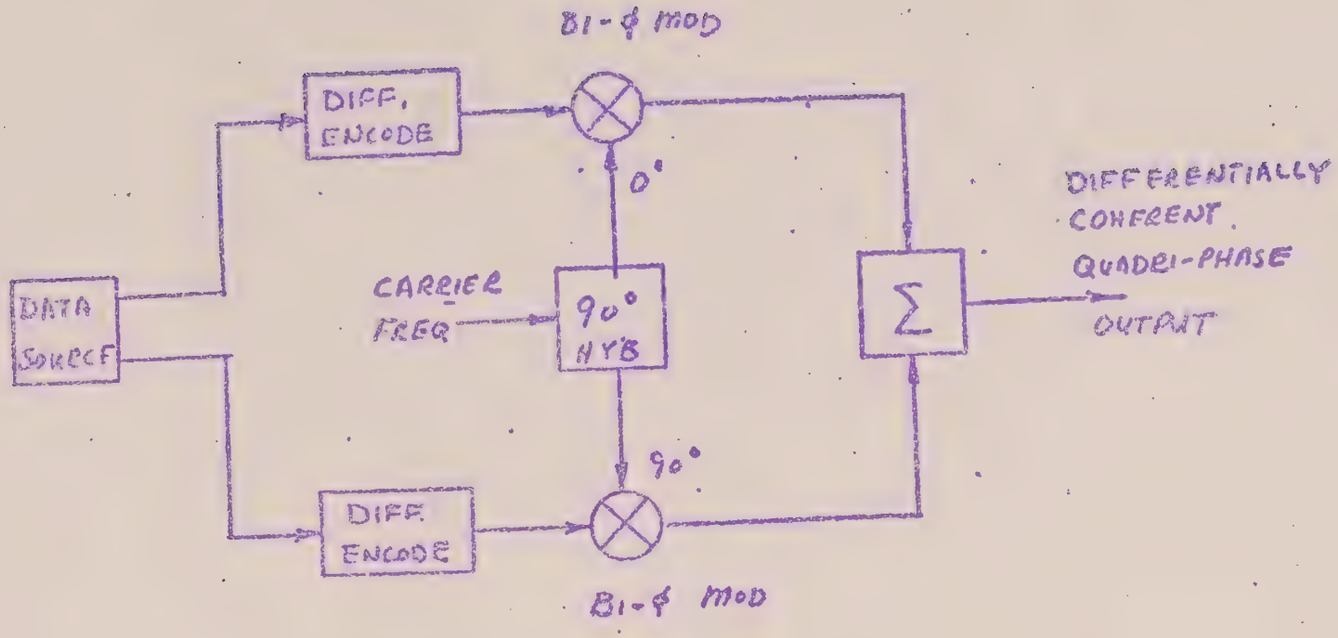
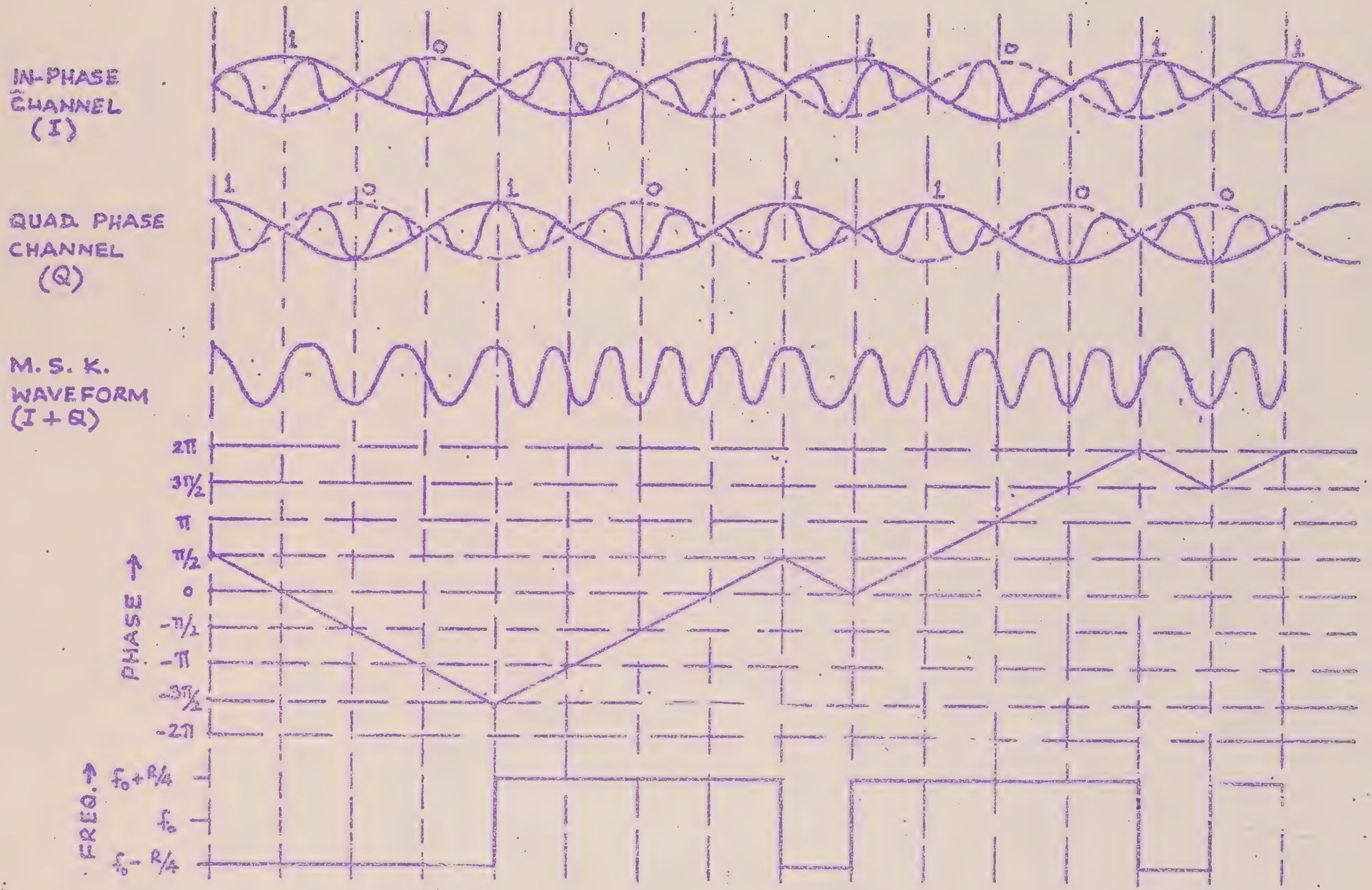


FIGURE 8 DC QUADRI-PHASE MODULATOR



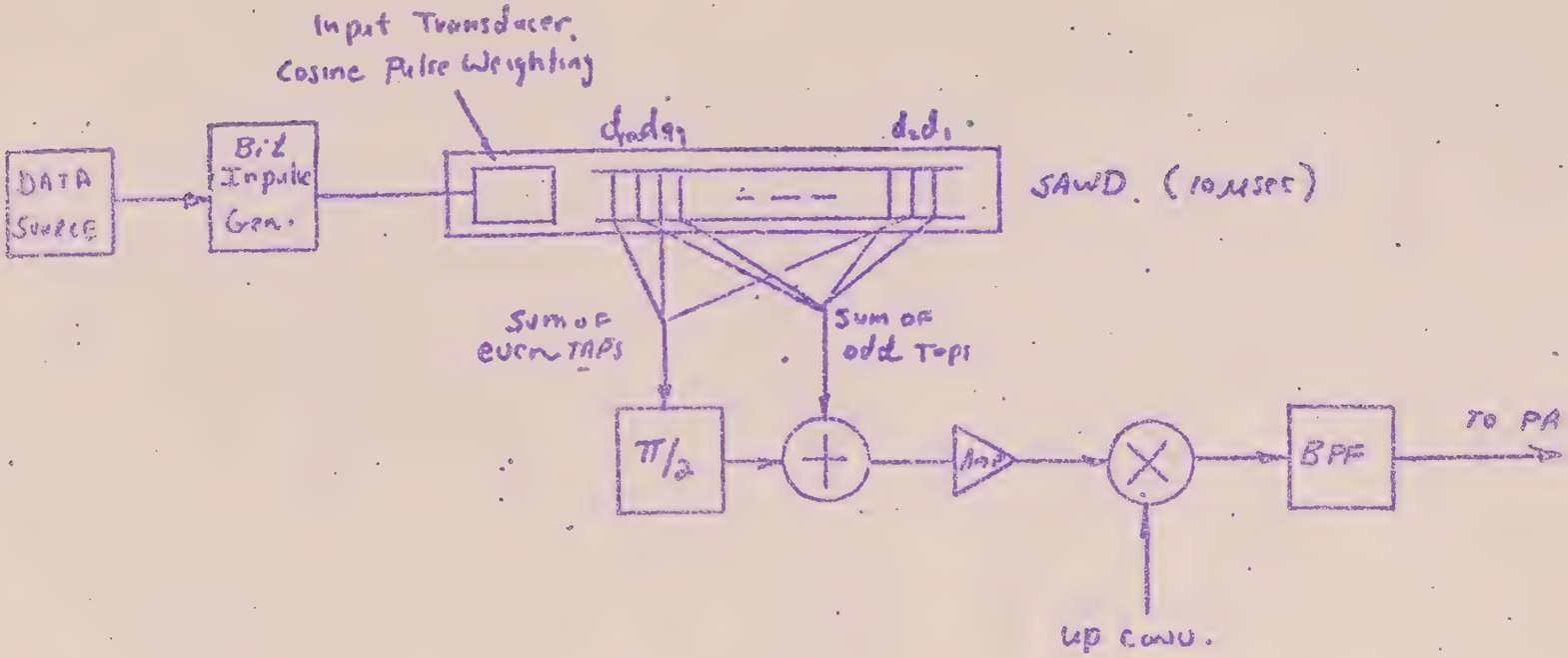
NORMALIZED FOR:

f_0 = 1 HZ

T_c = 1 second

CHIP RATE, $R = \frac{1}{4}$ HZ

FIG 9: M. S. K.



DATA BIT	OUTPUT CHIP SEQUENCE	
1	$S_1 = d_{100}\, d_{99} \cdots d_1$	$R(S_1 S_2) = -1$
0	$S_2 = -d_{100} - d_{99} \cdots - d_1$	

FIGARE 10 COHERENT MSK MODULATOR #1

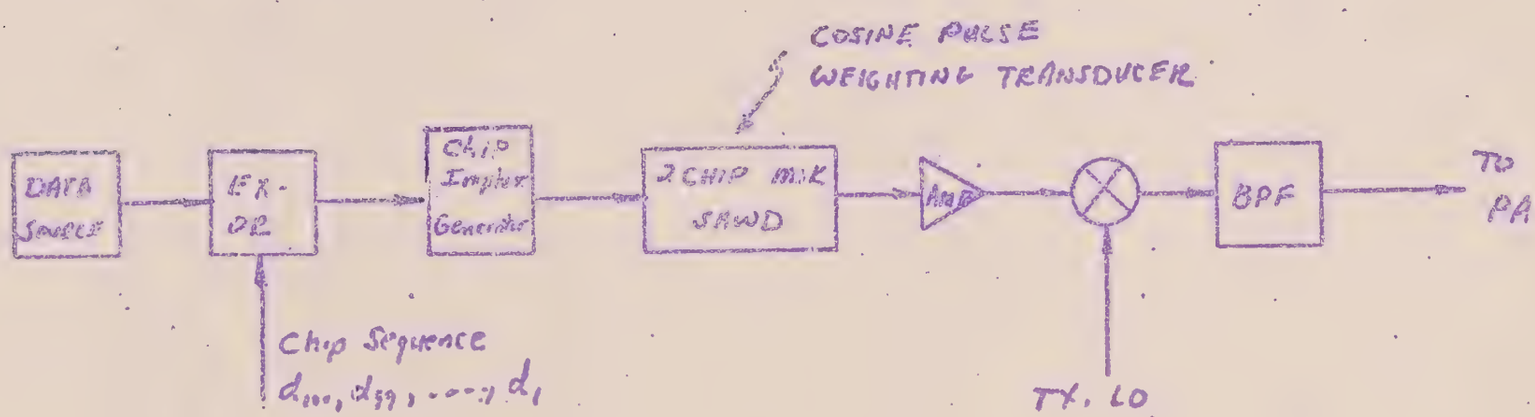


FIGURE 11 COHERENT MSK MODULATOR #2

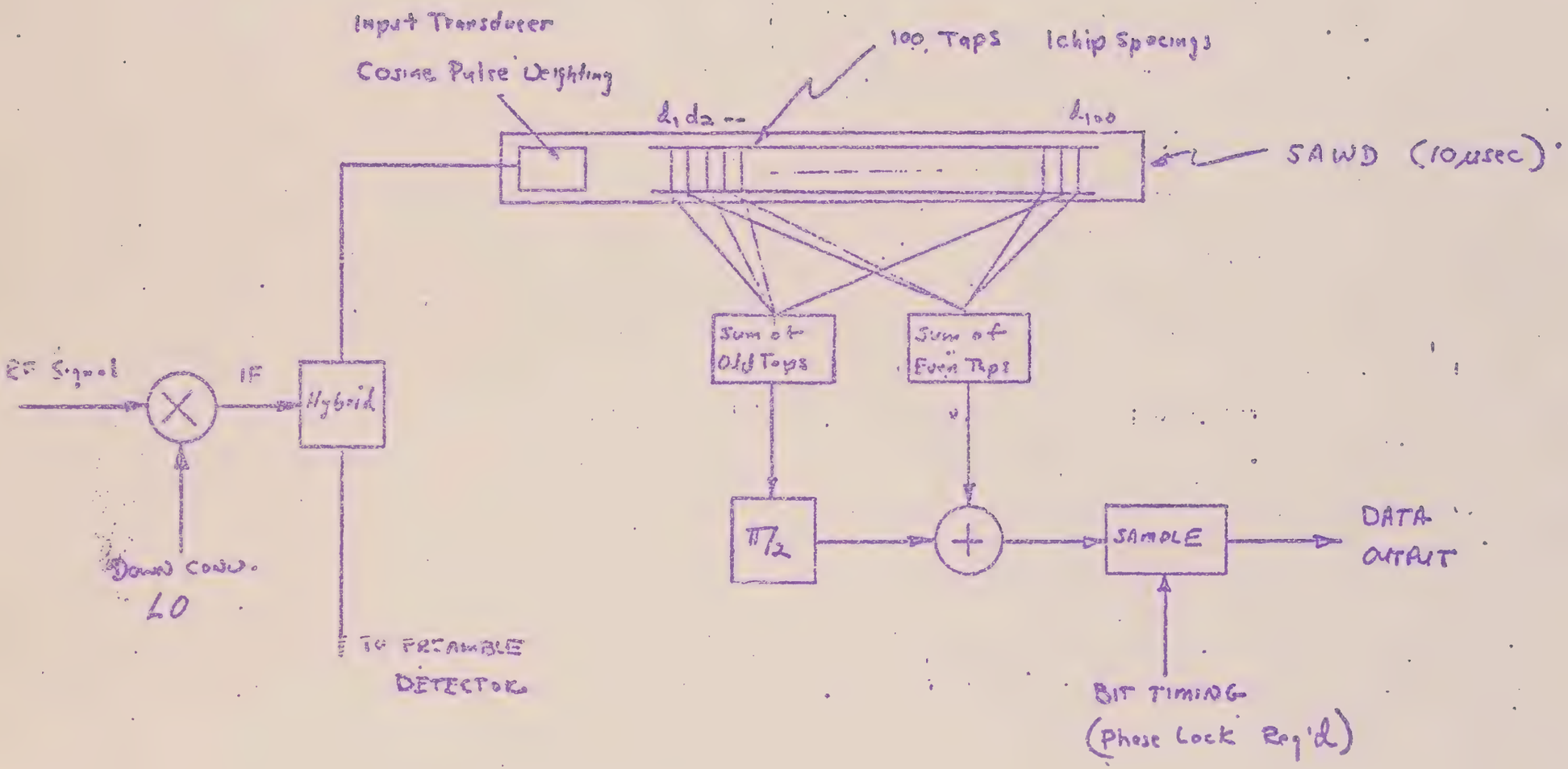


FIGURE 12 COHERENT MSK DEMODULATOR

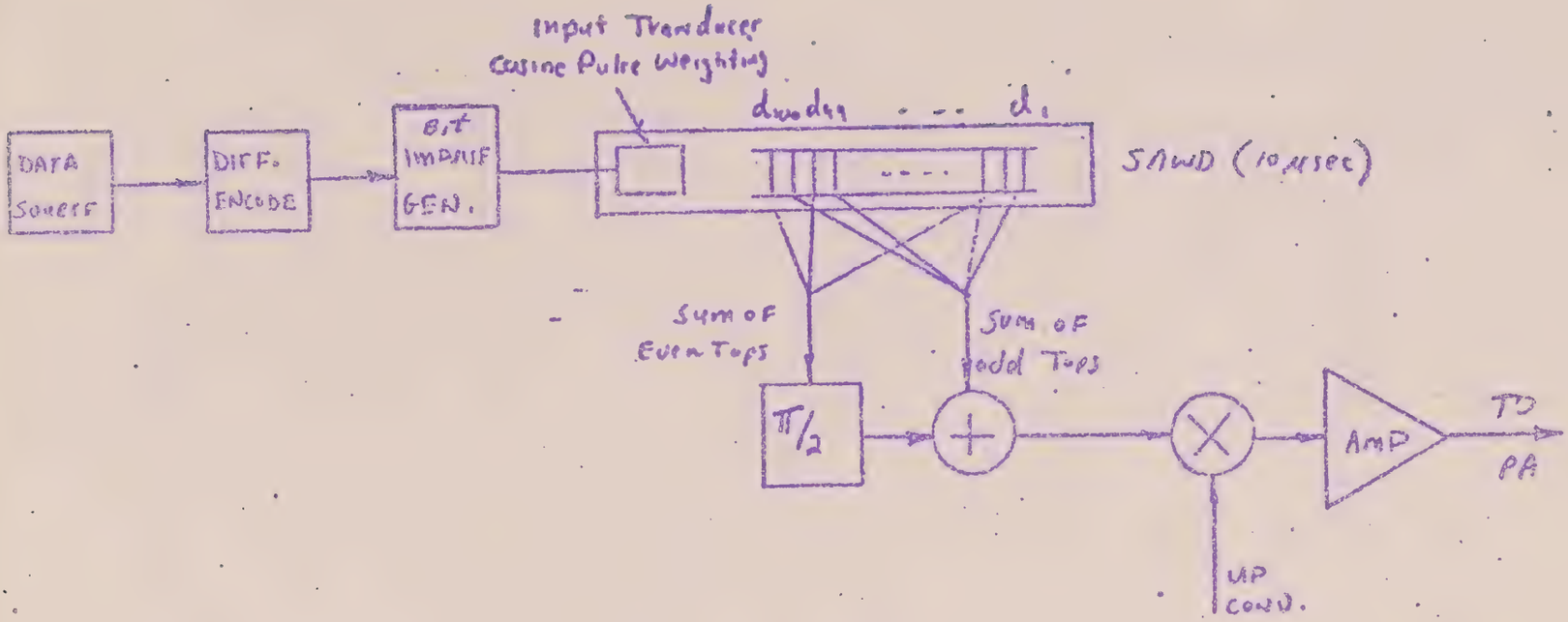


FIGURE 13 DIFFERENTIALLY COHERENT MSK MODULATOR.

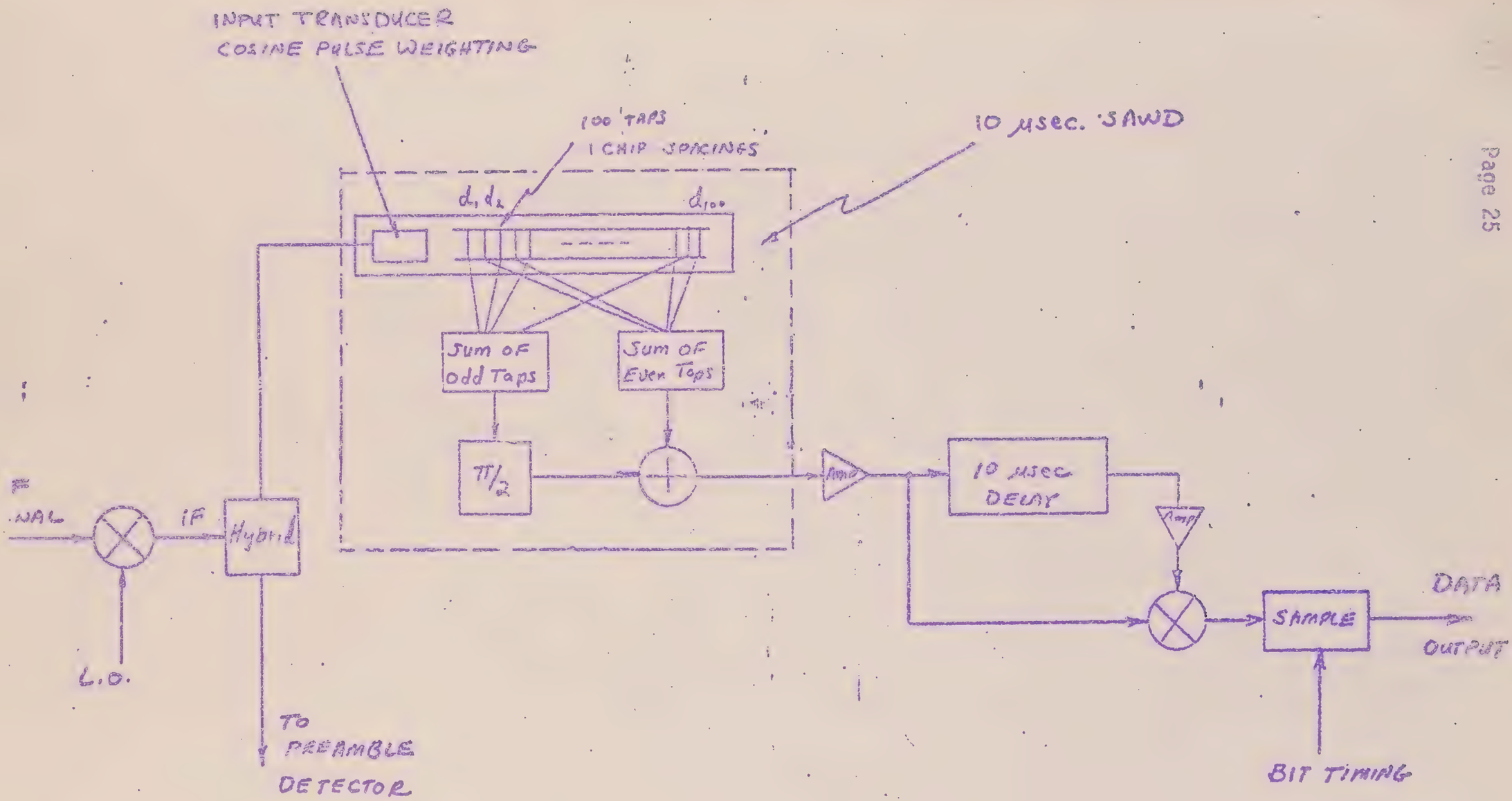


FIGURE 14A DIFFERENTIALLY COHERENT (DC) MSK DEMODULATOR

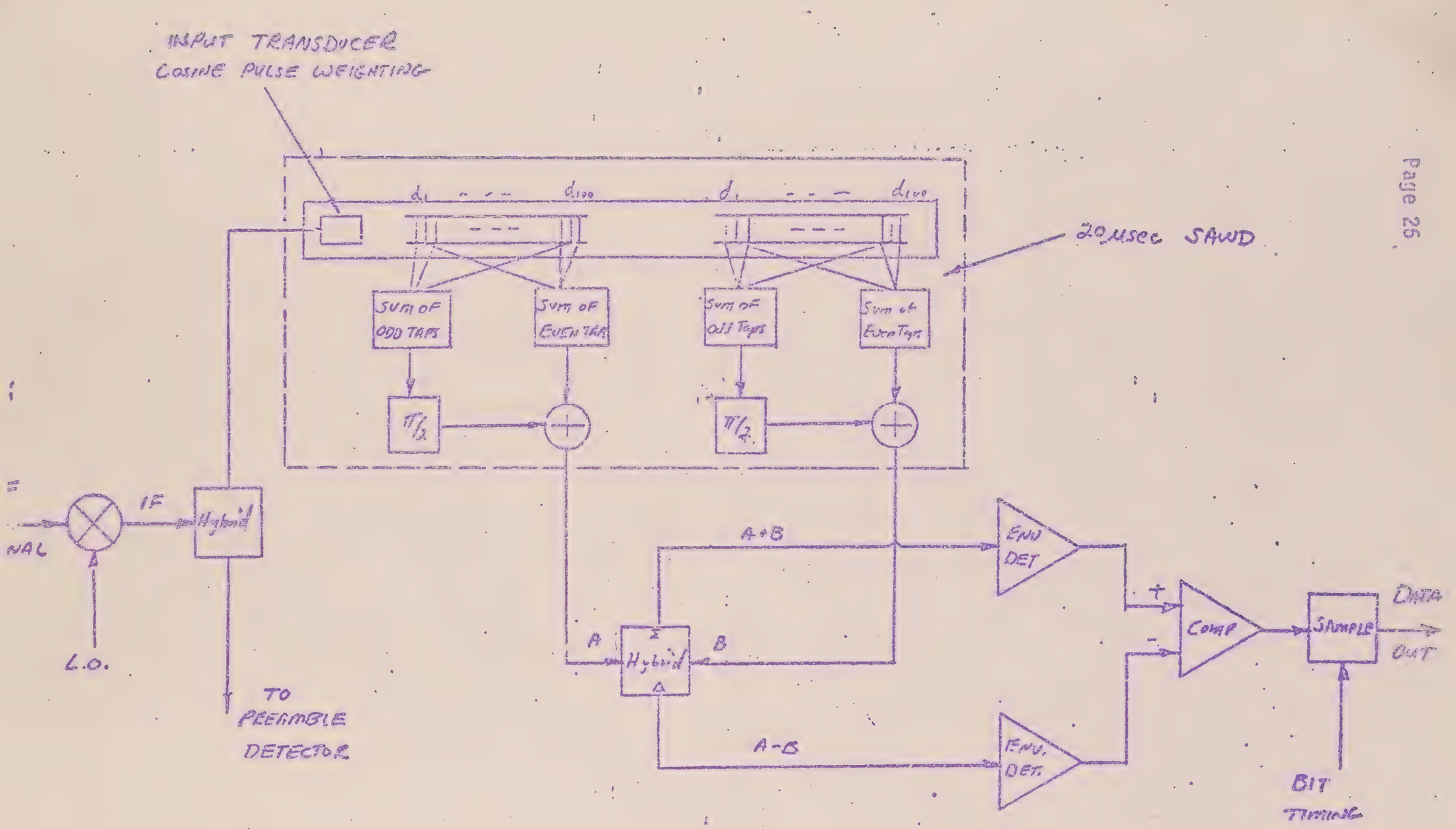
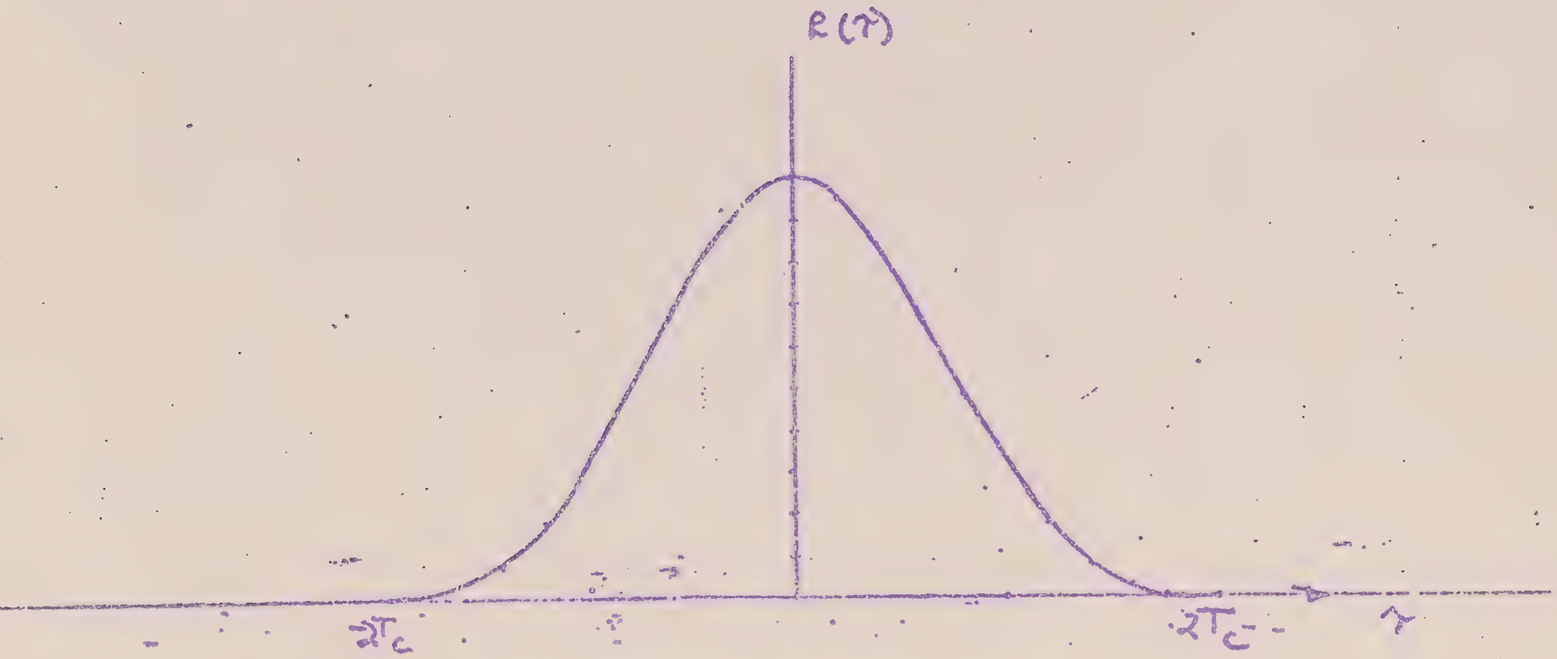


FIGURE 14B DIFFERENTIALLY COHERENT (DC) MSK DEMODULATOR

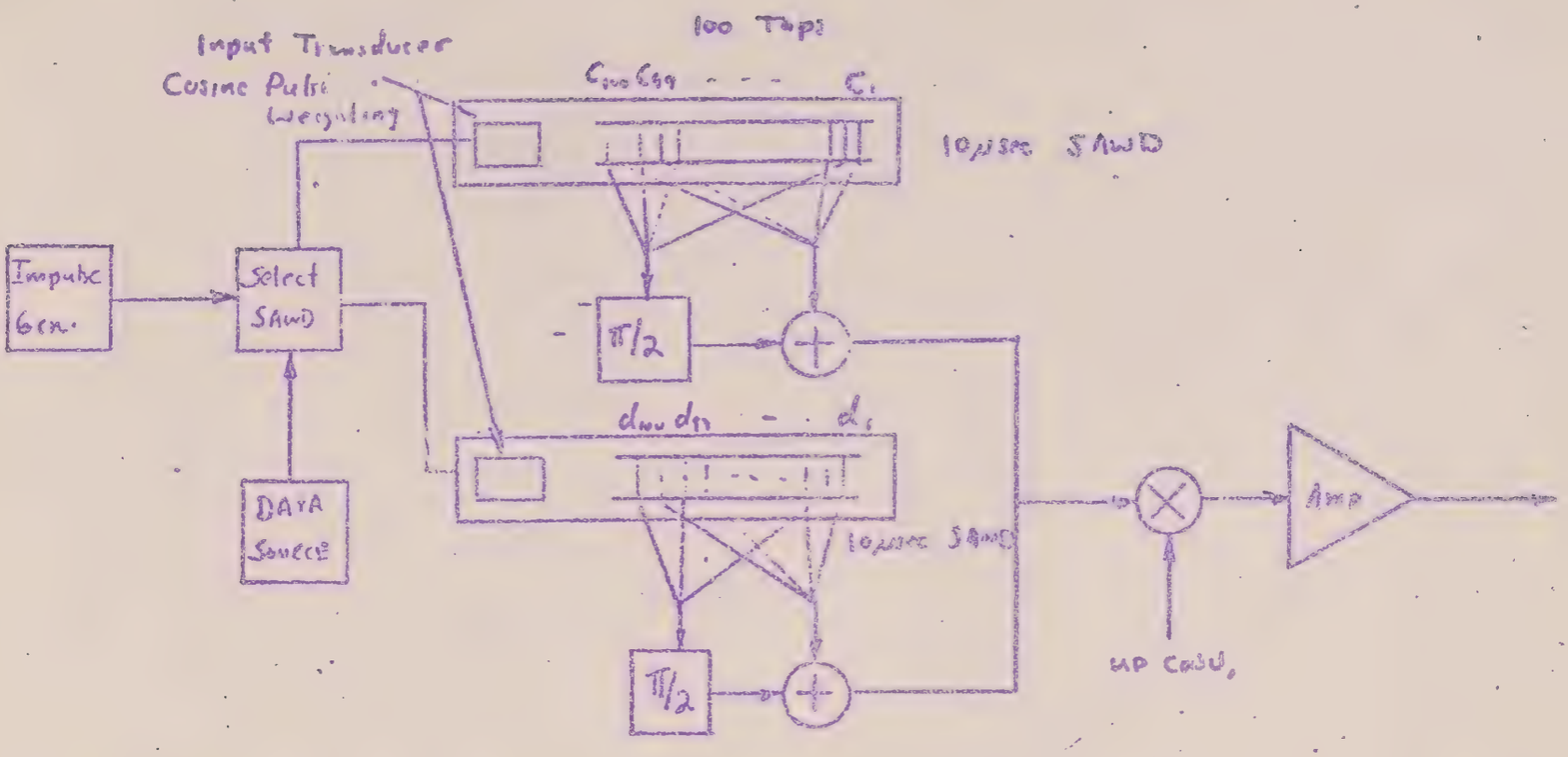
$$R(\tau) = \cos\frac{\pi t}{2T_c} * \cos\frac{\pi t}{2T_c}$$



SIGNAL AT OUTPUT OF MSK DETECTOR

$\tau/2T_c$	LOSS FACTOR (dB)	
0	0	IDEAL BIT TIMING
.05	.104	
.10	.41	
.20	1.58	
.30	3.49	
.40	6.23	
.50	9.95	

FIGURE 1: EFFECT OF TIMING OFFSETS FOR SAMPLING DETECTION OF MSK SIGNALLING



DATA BIT — OUTPUT CHIP SEQUENCE

1 — $S_1 = C_{100}\, C_{99} \cdots C_1$

0 — $S_2 = d_{100}\, d_{99} \cdots d_1$

$R(S_1, S_2) \approx 0$

FIGURE 16 PO MSK MODULATOR #1

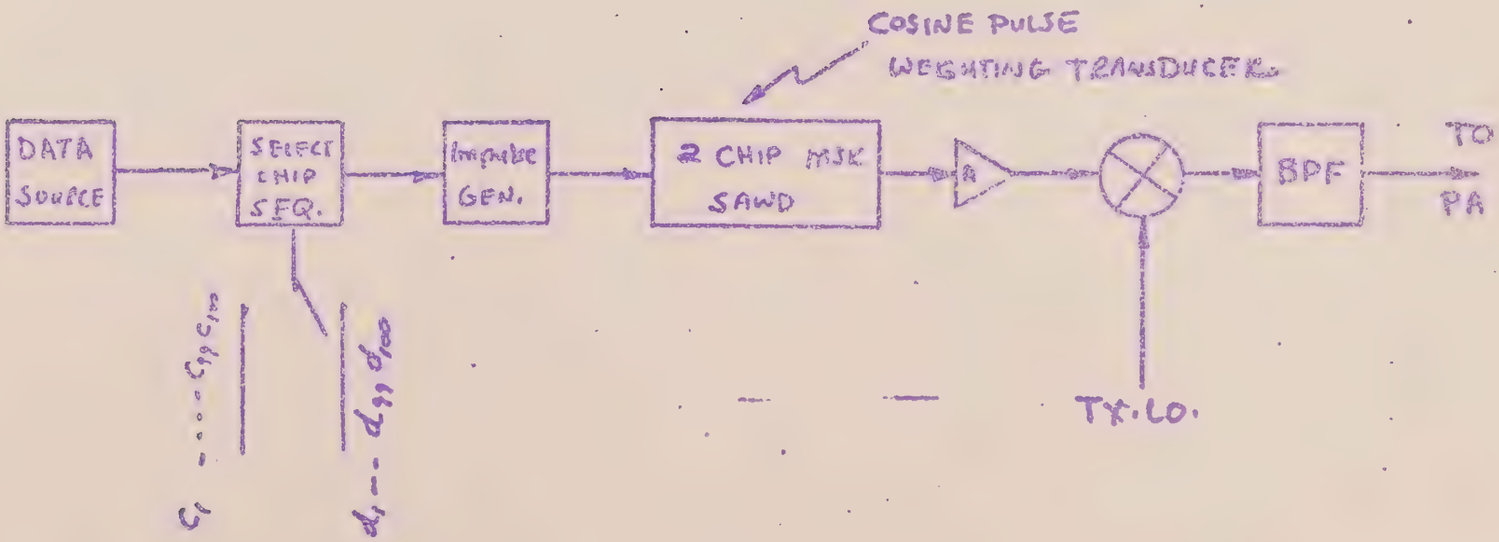


FIGURE 17 PO MSK MODULATOR #2

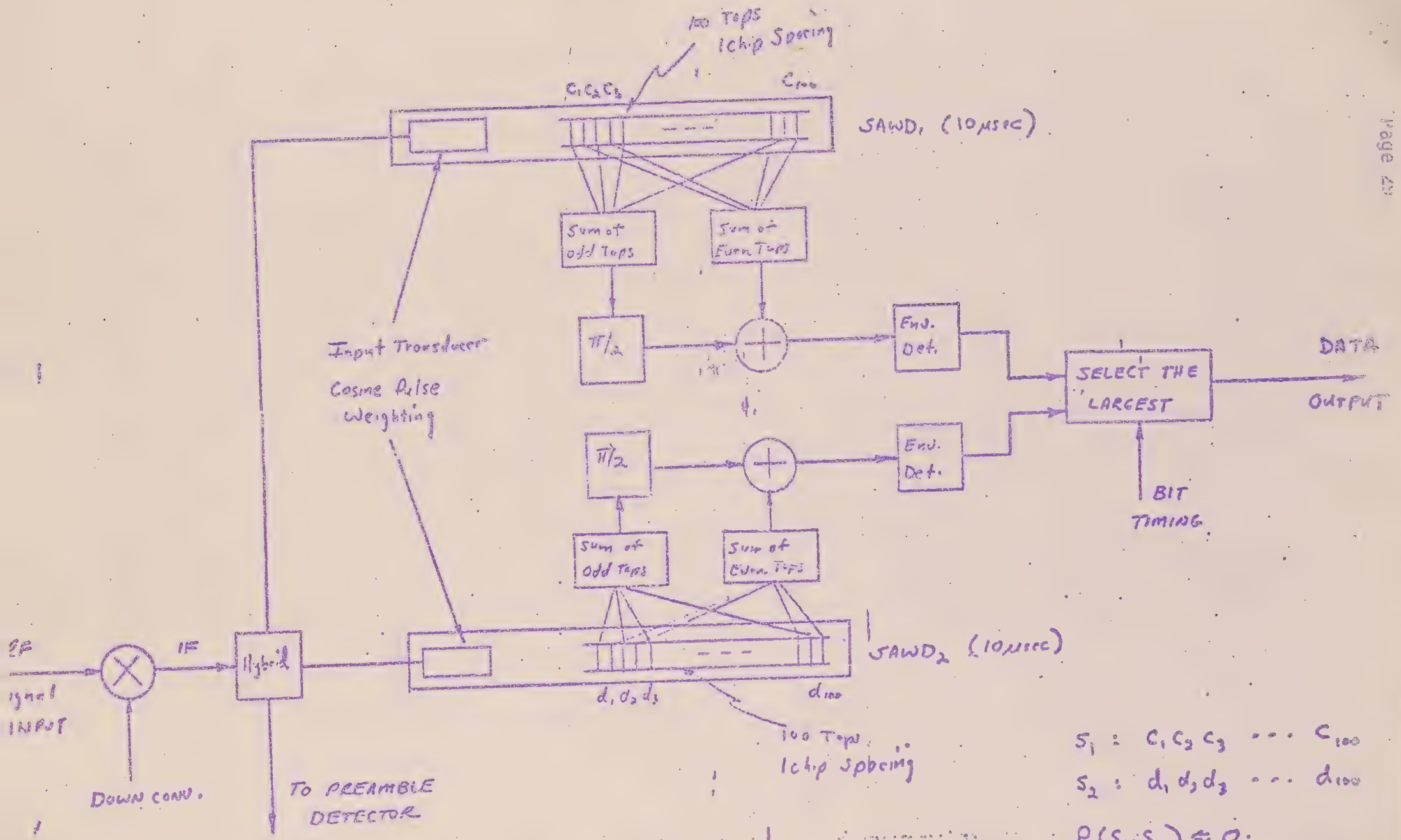
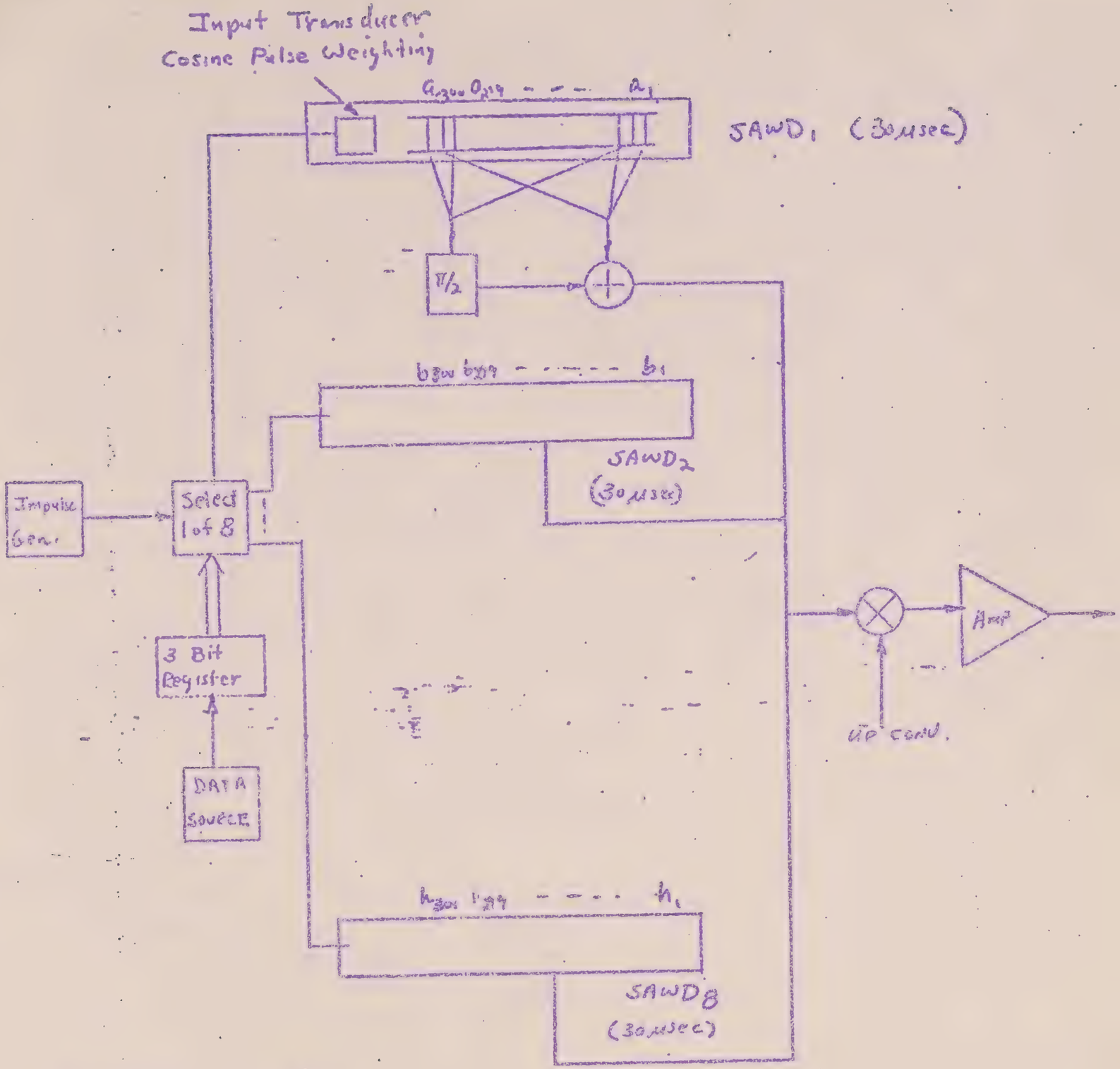


FIGURE 18 PO (Pseudo Orthogonal) MSK DEMODULATOR



S_1 : $a_1 a_2 \cdots a_{300}$

S_2 : $b_1 b_2 \cdots b_{300}$

⋮

S_8 : $h_1 h_2 \cdots h_{300}$

$$R(S_i S_j) = \delta_{ij}$$

where $\delta_{ij} = \begin{cases} 0 & \text{if } i \neq j \\ 1 & \text{if } i = j \end{cases}$

FIGURE 19 8 PSK MSK MODULATOR

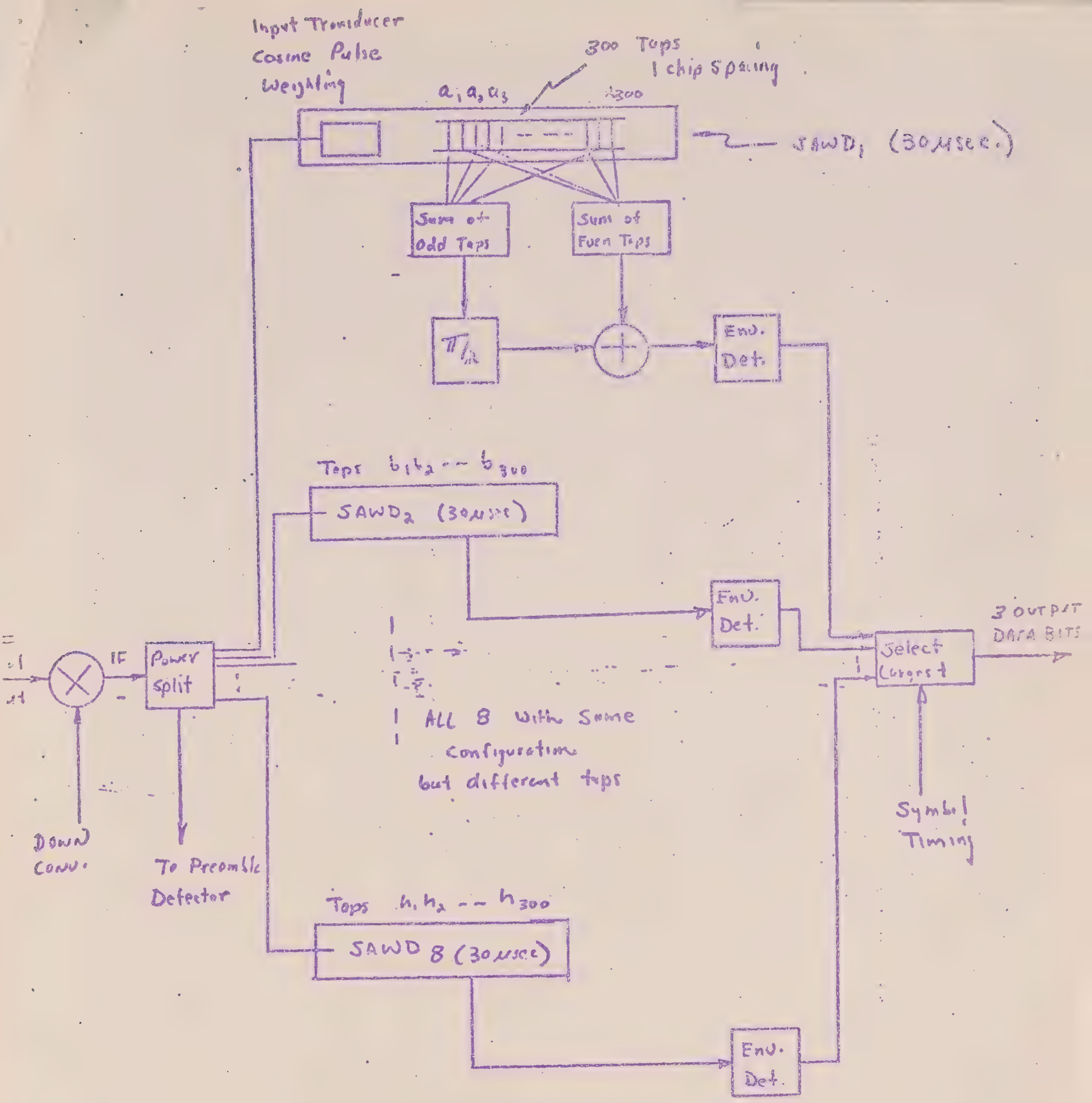


FIGURE 20 8'ARY MSK Demodulator

$S_1 : a_1 a_2 \cdots a_{300}$

$S_2 : b_1 b_2 \cdots b_{300}$

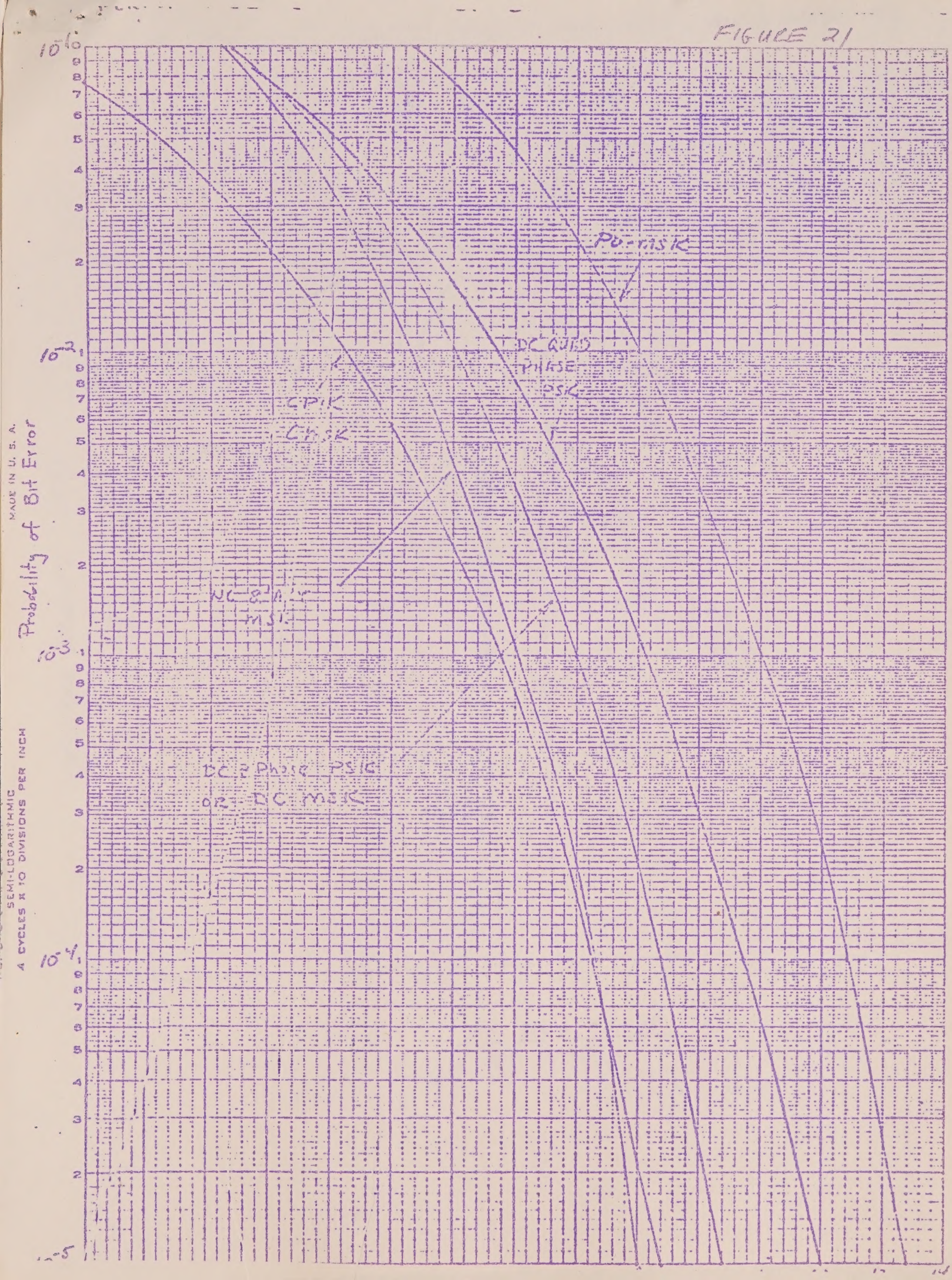
$\vdots$

$S_8 : h_1 h_2 \cdots h_{300}$

$R(S_i S_j) = \delta(i,j)$

where $\delta(i,j) = \begin{cases} \\ \end{cases}$

FIGURE 21


Probability of Bit Error
10⁻¹
10⁻²
10⁻³
10⁻⁴
10⁻⁵
Po-ras K
DC QPSK
PHASE
PSK
CPK
Cb SK
NC-8-PSK
MSK
DC 2 Phase PSK
OR DC MSK
MADE IN U. S. A.
SEMI-LOGARITHMIC
4 CYCLES X 10 DIVISIONS PER INCH

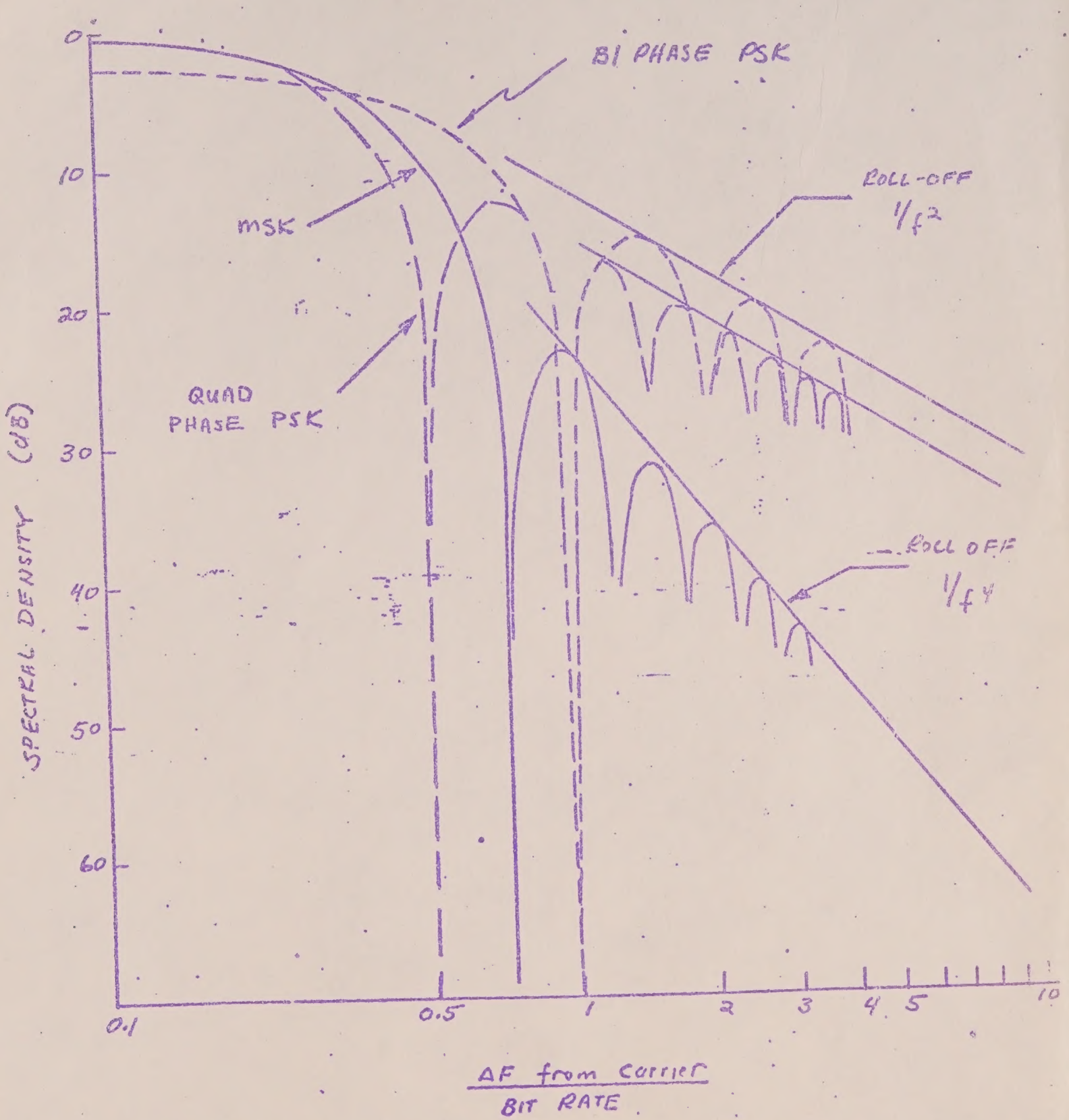



FIGURE 22 RELATIVE SPECTRAL DENSITY FOR MSK, QUAD PHASE PSK AND BI-PHASE PSK